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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,631	10/09/2003	Eric C. Pearson	03-0839-1496.00330	8431

24319 7590 03/12/2007

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EXAMINER	
ANYIKIRE, CHIKAODILI E	
ART UNIT	PAPER NUMBER
2621	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/682,631	PEARSON ET AL.	
	Examiner	Art Unit	
	Chikaodili E. Anyikire	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-20* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20040120*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to application number (10/682, 631) filed on October 09, 2003. Claims 1-20 are pending and have been examined.

Information Disclosure Statement

2. Acknowledgement is made of applicant's information disclosure statement

Specification

3. The disclosure is objected to because of the following informalities: The applicant failed to properly fill out section for the co-pending application (page 1, Ln 8).

The application has an error in its numerical order under the "Summary of Invention" (page 4, Ln 10-12).

Appropriate correction is required.

Claim Objections

4. Claim 7 is objected to because of the following informalities: the claim limitations are not recited in correct numerical order. There are two limitations numbered (iv). Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 11-15, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Auyeung et al (US 6, 813, 315).

As per claim 1, Auyeung et al discloses an apparatus (Fig 2) comprising:

a first memory (Fig 7, encoder 700, encoder 700 contains a frame memory for motion estimation) used for a motion estimation of a current block (Col 5, Ln 64-66); and

a circuit configured to (i) determine if a search window for said current block is at least partially outside a boundary of a picture (Fig 6c; it is seen by the figure that a search window does check outside the boundary of the picture) stored in a second memory (Fig 7, 720,Col 6, Ln 2-9),

(ii) copy a first plurality of reference samples in said search window from said second memory to said first memory (Col 6, Ln 10-48, the storage system holds the reference frames and transfers them to the video encoder during the process of motion estimation) and

(iii) map a plurality of reads from said first memory for a plurality of pad samples to said reference samples in said first memory, where said pad samples are determined to be outside said boundary (Col 4, Ln 5-12 and Col 6, Ln 10-48).

Regarding claim 11, arguments analogous to those presented for claim 11 is applicable to claim 11.

As per claim 12, Auyeung et al discloses further comprising the step of:

aligning a second plurality of said reference samples read from said first memory to a first plurality of current samples in said current block for comparison (Col 6, Ln 17 – 25, the comparison of digital image with that of the preceding is represented in Figs 6(a) – 6(f), 8, and 10).

As per claim 13, Auyeung et al discloses further comprising the step of:

aligning said pad samples with a second plurality of said current samples for comparison (Col 3, Ln 41-44 and Col 4, Ln 10-14, the applicant should note that the prior art uses reference samples to create padding samples, which are in turned used to compare the current samples).

As per claim 14, Auyeung et al discloses wherein said first plurality and said second plurality of said current samples comprise a 16 by 16 block (Col 2, Ln 56-57, it is a conventional procedure in MPEG compression standard).

As per claim 15, Auyeung et al discloses wherein step (B) comprises the sub-step of:

copying a number of blocks of said reference samples from said second memory (720) to said first memory (Col 6, Ln 10-48).

As per claim 16, Auyeung et al discloses wherein step (B) further comprises the sub-step of:

mapping an address of said number of blocks to align with said boundary (Fig 6a, Col 3, Ln 37-41 and Col 6, Ln 10-48, the search window which is used to map between a number of blocks along the boundary).

As per claim 18, Auyeung et al discloses wherein step (A) comprises the sub-step of:

determining a horizontal position of a block within said search window relative to said boundary (Figs 6(a)-6(f), these figures represent the process in which the search window operates relative to the boundary of frame and also Cols 3 and 4 give further detail about how the method functions).

As per claim 19, Auyeung et al discloses wherein step (A) further comprises the sub-step of:

determining a vertical position of said block relative to said search window after determining said horizontal position (Figs 6(a)-6(f), these figures represent the process in which the search window operates relative to the boundary of frame and also Cols 3 and 4 give further detail about how the method functions).

Regarding claim 20, arguments analogous to those presented for claim 20 is applicable to claim 20.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2-7 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auyeung et al (US 6, 813, 315) in view of Bellas et al (US 2003/0174252).

As per claim 2, Auyeung et al discloses wherein said determining if said search window is at least partially outside said boundary (Fig 6c; it is seen by the figure that a search window does check outside the boundary of the picture).

However, Auyeung et al does not explicitly teach a circuit comprising a control circuit.

In the same field of endeavor, Bellas et al teaches the DMA unit is used to generate up to three independent addresses that are fed to the memory subsystem. The DMA unit contains six 16-bit registers. These registers control the functionality of

the address generation by the DMA and can be written by the programmer. They are mapped to control registers so that they can be read and modified in a single clock cycle. There are three such registers sets, for a total of 18 registers ([0061], [0062], Ln 1-5 and [0069], Ln 1-2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with the DMA unit of Bellas et al. The advantage of the DMA unit of Bellas et al is the contents of the registers remain intact across different loops, so that the overhead time is minimized in a lot of cases.

As per claim 3, Auyeung et al discloses an apparatus for motion estimation (Fig 7).

However, Auyeung et al does not explicitly teach a control circuit comprises a state machine configured to generate a plurality of map addresses and a state signal in response to a position of a sub-window in said search window relative to said boundary.

In the same field of endeavor, Bellas et al teaches the DMA unit is used to generate up to three independent addresses that are fed to the memory subsystem. The DMA unit contains six 16-bit registers. These addresses can be either absolute or a pair of (x,y) coordinates in a 2-D space. These registers control the functionality of the address generation by the DMA and can be written by the programmer. They are mapped to control registers so that they can be read and modified in a single clock cycle. There are three such registers sets, for a total of 18 registers. The registers are as follow ([0061], [0062], Ln 1-5):

(i) the initial address in register A stores the address from which the DMA starts counting. This can be either an absolute 16-bit address (from 0 to N-1, where N is the memory size), or a (x, y) coordinate pair ([0063]).

(ii) the vector size in register N is the total size of the space that the DMA will cover. For example, N=256 in order to cover all the 16x16 pixels of a MB ([0064]).

(iii) The chunk size in register K is the size of the subvector that the DMA will cover before the value the skip is added to the current address register C. In the previous example, K=16 ([0065]).

(iv)The register S stores the stride that is added to C if the skip J is not applied. It can be either an absolute 16-bit 2's complement number or a pair of 2's complement numbers for the x and y directions. For the example, S=(8,0) if a set of 16 pixels are read from the memory, and the scan of the memory is row-wise ([0066]).

(v) The register J stores the skip that is added to C, when a chunk K has been scanned. For the example, J=(-16, 2), to jump to the next row ([0067]).

(vi) The register C contains the address of the pixel to be accessed. It can be updated by the DMA, or be set by the programmer (for example, when only a single memory access is needed) ([0068]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with the DMA unit of Bellas et al. The advantage of the DMA unit of Bellas et al is the contents of the registers remain intact across different loops, so that the overhead time is minimized in a lot of cases.

As per claim 4, Auyeung et al discloses a motion estimation apparatus (Fig 7) and a first memory.

However, Auyeung et al does not explicitly teach wherein said circuit comprises a control circuit configured to generate an address to read from said first memory in response to a search address.

In the same field of endeavor, Bellas et al teaches the DMA unit is used to generate up to three independent addresses that are fed to the memory subsystem. The DMA unit contains six 16-bit registers. These addresses can be either absolute or a pair of (x,y) coordinates in a 2-D space. These registers control the functionality of the address generation by the DMA and can be written by the programmer. They are mapped to control registers so that they can be read and modified in a single clock cycle. There are three such registers sets, for a total of 18 registers ([0061], [0062], Ln 1-5 and [0069], Ln 1-2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with the DMA unit of Bellas et al. The advantage of the DMA unit of Bellas et al is the contents of the registers remain intact across different loops, so that the overhead time is minimized in a lot of cases.

As per claim 5, Auyeung et al discloses a motion estimation apparatus (Fig 7).

However, Auyeung et al does not explicitly teach wherein said control circuit comprises:

a first circuit configured to generate an intermediate address in response to said search address; and

a second circuit configured to generate said address by comparing said intermediate address with one of a plurality of map addresses for a plurality of columns in said search window.

In the same field of endeavor, Bellas et al teaches the DMA unit is used to generate up to three independent addresses that are fed to the memory subsystem. The DMA unit contains six 16-bit registers. These addresses can be either absolute or a pair of (x,y) coordinates in a 2-D space. These registers control the functionality of the address generation by the DMA and can be written by the programmer. They are mapped to control registers so that they can be read and modified in a single clock cycle. There are three such registers sets, for a total of 18 registers. The registers are as follow ([0061], [0062], Ln 1-5):

(i) the initial address in register A stores the address from which the DMA starts counting. This can be either an absolute 16-bit address (from 0 to N-1, where N is the memory size), or a (x, y) coordinate pair ([0063]).

(ii) the vector size in register N is the total size of the space that the DMA will cover. For example, N=256 in order to cover all the 16x16 pixels of a MB ([0064]).

(iii) The chunk size in register K is the size of the subvector that the DMA will cover before the value the skip is added to the current address register C. In the previous example, K=16 ([0065]).

(iv)The register S stores the stride that is added to C if the skip J is not applied. It can be either an absolute 16-bit 2's complement number or a pair of 2's complement numbers for the x and y directions. For the example, S=(8,0) if a set of 16 pixels are read from the memory, and the scan of the memory is row-wise ([0066]).

(v) The register J stores the skip that is added to C, when a chunk K has been scanned. For the example, J=(-16, 2), to jump to the next row ([0067]).

(vi) The register C contains the address of the pixel to be accessed. It can be updated by the DMA, or be set by the programmer (for example, when only a single memory access is needed) ([0068]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with the DMA unit of Bellas et al. The advantage of the DMA unit of Bellas et al is the contents of the registers remain intact across different loops, so that the overhead time is minimized in a lot of cases.

As per claim 6, Auyeung et al discloses an apparatus (Fig 7).

However, Auyeung et al does not explicitly teach wherein said control circuit further comprises a third circuit configured to generate a plurality of flags in response to said search address relative to said boundary.

In the same field of endeavor, Bellas et al teaches the SRAMs that are used in the ME module are preferably single-ported, so as to minimize the physical size of the module. During the course of the SoAD computation, the memory is accessed from two

different addresses: this is how data are inserted into the systolic array for parallel computation. When the current MB is at the edges of the frame, the VMTU will convert the incoming addresses to the corresponding addresses within the frame and will attempt to access the appropriate SRAMs. In that case, a series of memory accesses that normally would have been made to N different SRAMs are collapsed to accesses in a smaller number of SRAMs. This entails more accesses per SRAM from different addresses ([0058]). To solve this problem, the ME memory system is equipped with four SRAMs (called boundary SRAMs) that are used to provide this extra output port. They store the first or last column of a frame depending on the position of the current MB in the frame. The storage of pixel data in the Boundary SRAMs is initiated from the system interface ([0059]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with Boundary SRAMs (Fig 5, 340) of Bellas et al. The advantage of the boundary SRAMs unit of Bellas et al is that it provides an extra output port.

As per claim 7, Auyeung et al discloses an apparatus (Fig 7).

However, Auyeung et al does not explicitly teach wherein said second circuit is further responsive to said flags that indicate one of (i) outside a left edge of said boundary, (ii) crossing said left edge, (iii) between said left edge and right edge of said boundary, (iv) crossing said right edge and (v) outside said right edge.

In the same field of endeavor, Bellas et al teaches the SRAMs that are used in the ME module are preferably single-ported, so as to minimize the physical size of the module. During the course of the SoAD computation, the memory is accessed from two different addresses: this is how data are inserted into the systolic array for parallel computation. When the current MB is at the edges of the frame, the VMTU will convert the incoming addresses to the corresponding addresses within the frame and will attempt to access the appropriate SRAMs. In that case, a series of memory accesses that normally would have been made to N different SRAMs are collapsed to accesses in a smaller number of SRAMs. This entails more accesses per SRAM from different addresses ([0058]). To solve this problem, the ME memory system is equipped with four SRAMs (called boundary SRAMs) that are used to provide this extra output port. They store the first or last column of a frame depending on the position of the current MB in the frame. The storage of pixel data in the Boundary SRAMs is initiated from the system interface ([0059]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with Boundary SRAMs (Fig 5, 340) of Bellas et al. The advantage of the boundary SRAMs unit of Bellas et al is that it provides an extra output port.

As per claim 8, Auyeung et al discloses an apparatus (Fig 7) wherein mapping of said pad samples from said reference samples (Col 4, Ln 10-14 and Col 6, Ln 10-48).

However, Auyeung et al does not explicitly teach said circuit comprises a control circuit configured to generate a plurality of signals.

In the same field of endeavor, Bellas et al teaches the DMA unit is used to generate up to three independent addresses that are fed to the memory subsystem. The DMA unit contains six 16-bit registers. These addresses can be either absolute or a pair of (x,y) coordinates in a 2-D space. These registers control the functionality of the address generation by the DMA and can be written by the programmer. They are mapped to control registers so that they can be read and modified in a single clock cycle. There are three such registers sets, for a total of 18 registers ([0061], [0062], Ln 1-5 and [0069], Ln 1-2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with the DMA unit of Bellas et al. The advantage of the DMA unit of Bellas et al is the contents of the registers remain intact across different loops, so that the overhead time is minimized in a lot of cases.

As per claim 9, Auyeung et al discloses an apparatus (Fig 7) configured to append said pad samples to at least one of said reference samples in response to said signals (Col 4, Ln 10 –14 and Col 6, Ln 10-48).

However, Auyeung et al does not explicitly teach a said circuit comprises a shifter circuit.

In the same field of endeavor, Bellas et al teaches the DMA unit is used to generate up to three independent addresses that are fed to the memory subsystem.

The DMA unit contains six 16-bit registers. These addresses can be either absolute or a pair of (x,y) coordinates in a 2-D space. These registers control the functionality of the address generation by the DMA and can be written by the programmer. They are mapped to control registers so that they can be read and modified in a single clock cycle. There are three such registers sets, for a total of 18 registers ([0061], [0062], Ln 1-5 and [0069], Ln 1-2). The register as follow: the register S stores the stride that is added to C if the skip J is not applied. It can be either an absolute 16-bit 2's complement number or a pair of 2's complement numbers for the x and y directions. For the example, S=(8, 0) if a set of 16 pixels are read from the example, S=(8, 0) if a set of 16 pixels are read from the memory, and the scan of the memory is row-wise ([0066]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation of Auyeung et al with the DMA unit of Bellas et al. The advantage of the DMA unit of Bellas et al is the contents of the registers remain intact across different loops, so that the overhead time is minimized in a lot of cases.

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auyeung et al (US 6, 813, 315) in view of Linzer et al (US 6, 108, 039).

As per claim 17, Auyeung et al discloses motion estimation method.

However, Auyeung et al does not explicitly teach wherein said number of blocks comprises a 3-vertical by 5-horizontal arrangement of said blocks.

In the same field of endeavor, Linzer et al teaches conventional video compression techniques, such as MPEG-1, MPEG-2, H.261, H.262 and H.263 use both spatial and temporal compression or "encoding". For example in MPEG-2, a to-be-compressed, i.e, "to-be-encoded" picture (herein, "picture" means frame or field as per MPEG parlance) is divided into macroblocks. Each marcoblock includes an array IxJ luminance blocks and of an array of KxL total blocks (i.e., including chrominance blocks), where each luminance or chrominance block has pixels (Col 1, Ln 26-32, it is a conventional procedure in MPEG compression standard).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to integrate the motion estimation method with the arrangement of Linzer et al. The advantage of Linzer et al is that it provides numerous choices as to the possible arrangement of the blocks.

Allowable Subject Matter

11. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Prior Art Cited

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,608,656 to Purcell et al is cited for the circuit utilized for motion estimation.

U.S. Patent 6,421,698 to Hong is cited for the components from the circuit utilized for motion estimation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chikaodili E. Anyikire whose telephone number is (571) 270-1445. The examiner can normally be reached on Monday to Friday, 7:30 am to 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571) 272 - 7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CEA

Mehrdad Dastouri

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TC 2600